REMARKS

The claims are claims 1 to 6.

The application has been amended to provide description of element 211 illustrated in Figure 2 and element 503 illustrated in Figure 5.

Claims 3 and 4 were rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The OFFICE ACTION states that the copying of the display list into the second memory recited in claim 3 is insufficiently supported in the specification as to why there is a need for the copying of the display list into the second memory.

The Applicants respectfully submit that the original application includes sufficient support to the recitations of claims 3 and 4. The original application states at page 12, lines 11 to 26:

> "Process 500 then transfers the parsed list of display elements for the current page and sub-band to SRAM 435 (processing block 504). Additional auxiliary data required to render these display element may also be transferred to the on-chip SRAM. This auxiliary data could be fonts, color tables and the like. These steps (processing blocks 502 and 503) store in data needed for rendering in SRAM 435. This serves to increase the rendering speed because of the high memory bandwidth between central processing unit 410 and SRAM 435."

This portion of the original application clearly states transfer of the display element to the second memory as recited in claim 3 and auxiliary data as recited in claim 4.

The Applicants dispute that 35 U.S.C. 112 requires that application describe the reasons for limitations recited in the claims. The Applicants respectfully submit that 35 U.S.C. 112 only requires a written description of how to make and use the

invention. The OFFICE ACTION does not allege the written description fails to teach how to make and use the invention. However, the final sentence of the above quoted portion of the original application states that the copying recited in claims 3 and 4 increases the rendering speed because of the high memory bandwidth of the second memory. Accordingly, claims 3 and 4 are proper under 35 U.S.C. 112.

Claims 1, 2, 5 and 6 are rejected under 35 U.S.C. 103(a) as made obvious by Ueda U.S. Patent No. 6,538,764.

Claim 1 recites subject matter that is not made obvious by Ueda. Claim 1 recites "a first memory having a first data size and a first data transfer rate and a second memory having a second data size smaller than the first data size and a second data transfer rate faster than the first data transfer rate" and "for each element of the display list rendering pixels within the current sub-band into a corresponding memory location within the second memory, following the rendering step, transferring pixel data from the second memory to corresponding memory locations within the current sub-band of the page buffer." The OFFICE ACTION states that Ueda fails to teach the first and second memories with differing data transfer rates. The OFFICE ACTION states at page 3, lines 17 to 22:

> "However, one skilled in the art knows the clear advantage of using a faster memory, that is, for faster processing of information. It would be obvious to one of ordinary skill in the art to just simply use a faster type of memory in place of the band buffer. Such techniques are well known in the computing environment and is similar to the idea of caching."

The advantage of a faster memory is well known as stated by the Examiner. Using a faster memory as the band buffer would be obvious. Claim 1 recites a different technique that this obvious

use of a faster memory. Claim 1 recites rendering pixels from each element of a display list for a band into the second memory, which is faster, and following the rendering transferring the pixel data into the first slower memory. This claimed method involves additional memory beyond that of the obvious use of a faster memory for the band buffer. The claimed technique requires the display band to be stored in the second memory, then transferred to the first memory, thus requiring more memory. The obvious use of a faster memory as a band buffer does not make obvious the use of two memories of differing speeds. The claimed method involves an additional data transfer than this obvious use of a faster memory. In the claimed method, data must be transferred from the second memory to the first memory. One skilled in the art would be lead to avoid addition memory transfers when attempting to speed operations. Claim 1 thus recites more memory and more data transfer operations than the obvious use of a faster memory for the band buffer. Accordingly, claim 1 is not made obvious by Ueda.

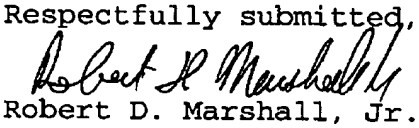
Claim 5 recites subject matter not made obvious by Ueda. Claim 5 recites "the digital processing system includes a partitionable memory selectively partitionable between cache and directly addressable memory" and that the method includes "prior to the rendering step for a first sub-band partitioning the partitionable memory to include directly addressable memory to serve as the second memory." The OFFICE ACTION cites RAM 13 illustrated in Figure 11 of Ueda as making obvious this partitioning. Ueda fails to teach that RAM 13 is selectively partitionable between cache and directly addressable memory. In fact, Ueda includes no teaching of cache. Therefore Ueda cannot make obvious partitioning a memory into directly addressable memory in contrast to cache memory. Thus claim 5 is not made obvious by Ueda.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

Texas Instruments Incorporated
P.O. Box 655474 M/S 3999
Dallas, Texas 75265
(972) 917-5290
Fax: (972) 917-4418

Respectfully submitted,



Robert D. Marshall, Jr.
Reg. No. 28,527